The Analysis of Inhomogeneous Barrier Height in In/SnTe/Si/Ag Diode

Araştırma Makalesi / Research Article

Hasan Hüseyin GÜLLÜ[1,2], Dilber Esra YILDIZ[3,*]

[1]Central Laboratory, Middle East Technical University, Ankara, Turkey
[2]Center for Solar Energy Research and Applications (GÜNAM), Middle East Technical University, Ankara, Turkey
[3]Faculty of Arts and Science, Department of Physics, Hitit University, Çorum, Turkey

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ABSTRACT

SnTe thin film layer was fabricated by magnetron sputtering technique on n-Si substrate, and the electrical properties of the In/SnTe/Si/Ag diode structure was investigated by using temperature dependent forward bias current-voltage (I-V) measurements. The main diode parameters were calculated according to the thermionic emission (TE) model and they were found in an abnormal behavior with change in temperate in which zero-bias barrier height (Φ_{B0}) increases and ideality factor (n) decreases with increasing temperature. Therefore, the total current flow though the junction was expressed by the Gaussian distribution (GD) of barrier height. The plot of Φ_{B0} vs $q/2kT$ showed the existence of inhomogeneous barrier formation and evidence for the application of Gaussian function to identify the distribution of low barrier height patches. The mean barrier height was found as 1.274 with the 0.166 eV standard deviation. From the modified Richardson plot, Richardson constant was calculated as 119.5A/cm^{2}K^2 in very close agreement with the reported values. Additionally, the effects of the series resistance (R_S) were analyzed by using Cheung's function. Distribution of the interface states (D_{it}) were extracted from the I-V characteristics and found in increasing behavior with decreasing temperature.

Keywords: Sputtering technique, barrier height, Gaussian distribution, interface states.

In/SnTe/Si/Ag Diyotunda Homojen Olmayan Engel Yüksekliği Analizi

ÖZ

SnTe ince film katmanı magnetron saçtırma tekniği ile n-Si alttaş üzerine büyütüldü, ve In/SnTe/Si/Ag diyot yapısının elektriksel özellikleri, sıcaklık bağımlı düz besleme akım-voltaj (I-V) ölçümleri kullanılarak incelendi. Temel diyot parametreleri termiyonik emisyon (TE) modeli temel alınarak hesaplandı ve sıcaklık artışı ile sıfır-potansiyel engel yüksekliğinin (Φ_{B0}) artışı ve idealite faktörünün (n) azalışı gibi ideal olmayan bir davranışta oldukları bulundu. Bu nedenle, eklemdeki toplam akım iletimi, engel yüksekliğinin Gauss dağılımı (GD) ile açıklandı. Φ_{B0} vs $q/2kT$ eğrisi, yapıdaki homojen olmayan engel oluşumunu ve GD kullanılarak düşük bariyerli local bölgelerin dağılımının açıklanabileceğini gösterdi. 0.166 eV standart sapma ile birlikte ortalama engel yüksekliği 1.274 eV olarak bulundu. Etkin Richardson eğrisinden, Richardson sabiti, literatürdeki değerlere yakın bir değerde, 119.5A/cm^{2}K^2 olarak hesaplandı. Ayrıca, Cheung fonksiyonu kullanılarak yapıdaki seri direnç (R_S) etkisi analiz edildi. Arayüzey durumların yoğunluğu (D_{it}) diyot yapısının I-V karakteristiğinden elde edildi ve azalan sıcaklık değerlerine göre artış yönünde bir davranış gösterdiği bulundu.

Anahtar Kelimeler: Saçturma tekniği, engel yüksekliği, Gauss dağılımı, arayüzey durumları

1. INTRODUCTION (GİRİŞ)

In recent years, chalcogenide Sn-based thin film structures have attracted considerable interest due to their promising properties in a wide range of device applications including microelectronics, batteries and photovoltaics [1, 2]. Especially, these binary IV–VI compounds have been point of interest due to their electrical and optical properties. Although there arestandard current-voltage (I-V) analysis under the consideration of determining intrinsic and contact

parameters of Si-based diode structures, SnS, SnSe and SnTe have generated a great deal of interest as an important narrow band gap IV–VI layered compounds for efficient solar energy conversion through solar cells [5,6]. According to the concern in supply of constituent elements in large scale applications, their major advantage is the abundance of Sn [7]. Among these new compounds (SnSe and SnS), for efficient solar energy conversion through solar cells, SnTe have a great potential in device applications to construct high-performance, broadband photodetectors with a spectrum range from ultraviolet to infrared [8]. Although SnTe thin film layer can be evaluated as a candidate on photovoltaic device applications with its large photocurrents responsivity, it has been popular as a topological crystalline insulator in photodetectors for near-infrared detection [8-10].

*Sorumlu Yazar (Corresponding Author)
e-posta : desrayildiz@hitit.edu.tr

In this work, SnTe thin film layer was deposited on mono-crystalline n-Si wafer substrate by magnetron sputtering technique. Since Si has been widely used in photovoltaic devices, photodetectors, and imaging devices, In/SnTe/Si/Ag structure was introduced as a preliminary step toward forming a SnTe-based diode. In a better understanding of electrical properties of this structure, experimental investigation was focused on the temperature dependence of I-V characteristics of In/SnTe/Si/Ag structure.

2. MATERIAL and METHOD (MATERYAL VE METOD)

The In/SnTe/Si/Ag structure was fabricated by sputtering of SnTe film layer on 600 μm thick, (111) oriented n-type (P-doped) crystalline Si wafer with the resistivity value of 1-10 (Ω-cm). Before deposition processes, Si substrates were chemically etched to remove native oxide and then rinsed in deionized water. The back ohmic contact on the Si wafer was formed by elemental Ag evaporation onto the whole back surface of the wafer and subsequent annealing treatment at 450°C under the nitrogen atmosphere. The SnTe film was deposited on n-Si wafer substrate using RF magnetron sputtering system from a high-purity SnTe target. During the deposition process, the substrate temperature was kept constant at 200°C and the deposition rate was controlled at around 1.0 Å/s. The rate and thickness values were monitored and controlled by Inficon XTM/2 deposition monitor and the final thickness was measured by Vecoo Dektak 6M thickness profilometer. Atomic composition of the film layer was determined by Quanta 400 FEG model scanning electron microscope (SEM) equipped with energy dispersive X-ray spectroscopy (EDS) system. The surface morphology of thin films was monitored by means of AFM analysis using Veeco Multimode V. Electrical characteristics of the film was evaluated by using Keithley 2400 sourcemeter to apply bias voltage and also to measure the resultant current.

In addition, a shadow mask in circular dot contact shape of 2 mm diameter was used to deposit 200 nm In top contact layer onto SnTe film surface by thermal evaporation; then the complete structure was annealed at 100°C under the nitrogen atmosphere. The diode characteristics were analyzed by temperature dependent I-V using a Keithley 2401 sourcemeter as a source/measure unit and CTI-Cryogenics Model 22 refrigerator system combined with Model SC helium compressor to scan the diode temperature from 220 to 360 K with the help of Lakeshore DRC-91C controller.

3. RESULTS AND DISCUSSION (SONUÇLAR VE TARTIŞMA)

From EDS analysis, the chemical composition of the film confirms the presence of Sn and Te in the structure with a stoichiometric composition in 1:1 ratio of component elements. The final thickness of the deposited film layer was measured by profilometer and it was found as about 350 nm. AFM morphological surface characterization is used to study the surface of the thin film and it was observed as being a smooth, compact, and densely packed morphology. In addition, AFM imaging reveals that the root-mean-square (RMS) roughness of the film surface was about 1.66 nm. From the XRD spectrum of the film, deposited film layer was found in polycrystalline structure along (111) orientation direction exhibiting cubic crystal geometry [9]. Applying four-point probe technique, I-V measurements at room temperature showed that the deposited film layer is in high resistive characteristics with the value of about 10^2 Ω.cm.

The experimental forward and reverse bias I-V characteristics of the In/SnTe/Si/Ag diode carried out at the ambient temperature range of 220-360 K under dark condition is presented as semi-logarithmic I-V plot in Fig.1.

I-V measurements are used in order to investigate the rectifying behavior of the fabricated diode, determine the main diode parameters ad identify the conduction mechanisms in current transport through the junction. From Fig.1, the rectifying behavior in I with V can be evaluated as an indication of a typical junction diode [11] and these characteristics show about two order in magnitude of rectification factor (ratio of forward to reverse current).

Table 1. Calculated diode parameters of In/SnTe/Si/Ag diode by using TE model

Temperature (K)	Ideality factor (n)	Saturation current (I_0)	Barrier Height (Φ_{B0})
360	1.928	$6.39\text{x}10^{-7}$	0.827
340	2.080	$3.05\text{x}10^{-7}$	0.799
320	2.440	$8.67\text{x}10^{-8}$	0.783
300	3.350	$4.70\text{x}10^{-8}$	0.747
280	3.926	$4.22\text{x}10^{-8}$	0.696
260	4.196	$2.11\text{x}10^{-8}$	0.659
240	5.096	$1.88\text{x}10^{-8}$	0.607
220	5.769	$1.23\text{x}10^{-8}$	0.561

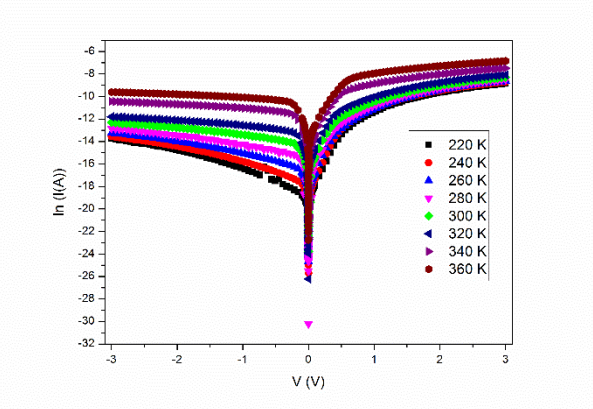

Figure 1. Semi-logarithmic I-V plots of In/SnTe/Si/Ag diode at different ambient temperatures

The current through the junction barrier at forward bias region can be expressed with the deviation from ideality as;

$$I = I_0 \left[exp\left(\frac{qV}{nkT}\right) - 1 \right] \quad (1)$$

where I_0 is the reverse-saturation current, q is the electronic charge, V is the voltage value in the forward bias region, k is the Boltzmann constant, n is the ideality factor and T is the diode temperature. This expression was applied in the case of $V > 3kT/q$ in order to neglect the reverse current contribution [12]. According to the thermionic emission (TE) theory, unity in n corresponds to the ideal case, on the other hand, a deviation from pure TE model is usually observed in which $n > 1$ indicates the contribution of the other conduction mechanisms to the carrier transport in the junction region.

The temperature dependent I-V analysis was carried out under the assumption of predominant effect of TE to determine the diode parameters of the In/SnTe/Si/Ag diode, as Φ_{B0}, n and I_0, as a function of temperature. Therefore, Io values were calculated at forward bias region under the assumption of homogeneous barrier height as,

$$I_0 = AA^*T^2 exp\left(\frac{-q\Phi_{B0}}{kT}\right) \quad (2)$$

where A is the effective diode area and A^* is the effective Richardson constant, Φ_{B0} is the barrier height at zero bias point. With TE assumptions on I-V behavior, A^* can be described according to the nearly free electrons in vacuum and it is reported as 112 A/cm^{2}K^2 for n-Si [11]. By using Eq.2, I_0 values were obtained from the straight line intercept value of $ln(I)$ at zero-applied voltage for each temperature step and tabulated in Table 1.

Based on TE model, the apparent Φ_{B0} values were estimated at each temperature according to the Richardson constant of n-Si layer from Eq.2. As listed in Table 1, these values show an abnormal behavior in which they are directly proportional to change in temperature. This temperature dependence indicates the inhomogeneous barrier formation in the diode, and the current flow can be explained by the existence of low barrier height patches [13,14]. In this case, charge carriers gain enough energy to overcome the higher barrier with increase in ambient temperature whereas they can pass over the lower barriers that triggers the current flow through patches having lower barrier height [15]. Therefore, this barrier differences over the whole temperature can be explained with TE modified under the consideration of barrier inhomogeneity.

n is evaluated as an expression of the barrier in the diode structure which is expected to be uniform for homogenous barrier formation and increases for an inhomogeneous barrier [16]. According to the Eq.1, it can be written as,

$$n = \frac{q}{kT}\left(\frac{dV}{dln(I)}\right) \quad (1)$$

The values were calculated from the slope of the linear region of the forward bias semi-logarithmic I-V plot, and found as to be greater-than-unity which indicates non-ideal diode behavior deviated from TE (Table 1). The high value of n can be attributed to presence of a particular distribution of interface states localized at the junction interface and barrier inhomogeneties with a wide distribution of low barrier patches [15, 17]. Consideration of the deformation of the barrier distribution and thus modifying TE model can explain the behavior of n with temperature.

The higher values of n can be evaluated as a result of the deformation of spatial barrier distribution when a bias voltage is applied and related to this fact, a linear correlation between Φ_{B0} and the n dependent on temperature as shown in Fig.2 [18]. As listed in Table 1, Φ_{B0} decreases and n increases, with increase in temperature. It was approximated by an examination of the degree of barrier height variation under the consideration of Tung's model and a linear relationship between Φ_{B0} and the n [19]. The extrapolation of the straight line shown in Fig.3 for $n = 1$ indicates a homogeneous barrier height around 0.88 eV. As a result, the decrease of Φ_{B0} and increase of the n especially at lower temperatures can be explained by the possible causes depending on the inhomogeneity in barrier height [20]. The same behavior of the ideality factor is observed in the literature and has been interpreted in terms of interface state density distribution (D_{it}) [21].

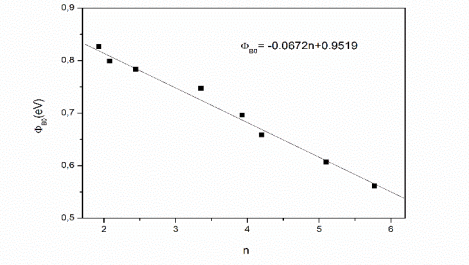

Figure 2. Barrier height vs. ideality factor for In/SnTe/Si/Ag diode

The obtained non-ideal I-V characteristics in TE theory can be analyzed by considering the fluctuations due to the barrier inhomogeneity and suggesting Gaussian distribution (GD) in barrier height, Φ_B [13-15]. This model estimated to analyze the transport properties of In/SnTe/Si/Ag diode, helps to explain the barrier differences and also n with their temperature dependence. According to the Werner's model, these observed potential fluctuations is assumed to be a continuous barrier distribution at the interface [22]. In this approach, the diode with Φ_B was approximated to be made of parallel diodes with different barrier heights which effect the current transport in the junction independently [14]. Therefore, the total current flow through the barrier at forward bias can be re-written as,

$$I = AA^*T^2 exp\left[\left(-\frac{qV}{kT}\right)\left(\bar{\Phi}_{B0} - \frac{q\sigma_0^2}{2kT}\right)\right] \times exp\left(\frac{qV}{n_{sp}kT}\right)\left[1 - exp\left(-\frac{qV}{kT}\right)\right] \quad (4)$$

with modified reverse saturation current expression as,

$$I_0 = AA^*T^2 exp\left(-\frac{q\Phi_{ap}}{kT}\right) \quad (5)$$

In this relation given in Eq.4, barrier height distribution is expressed in terms of Gaussian function with a standard deviation around a mean $\bar{\Phi}_{B0}$ and standard deviation σ_0 in temperature dependence of barrier height. In addition, σ_0 is used to measure the deviation from the homogeneity of barrier height in the junction [14], and Φ_{ap} and n_{ap} are the apparent barrier height and apparent ideality factor, respectively.

By using the Gaussian function to explain the inhomogeneous barrier height formation in the diode, the temperature variation of Φ_{B0} distribution can be represented as,

$$\Phi_{ap} = \bar{\Phi}_{B0} - \frac{q\sigma_0^2}{2kT} \quad (6)$$

from the modified barrier height expression [24]. The Φ_{B0} vs $q/2kT$ (Fig.8) indicates the expected linear relation given in Eq.6 and from the intercept and slope, $\bar{\Phi}_{B0}$ and σ_0 were calculated. The value of σ_0 is found to be 0.166 eV which is about 13% of $\bar{\Phi}_{B0}$, 1.274 eV. It shows that the investigated the fabricated In/SnTe/Si/Ag diode has an interfacial layer with inhomogeneities having a GD of barrier heights [22]. The single straight line observed in Fig.3 also verifies a presence of a single GD of barrier height [15].

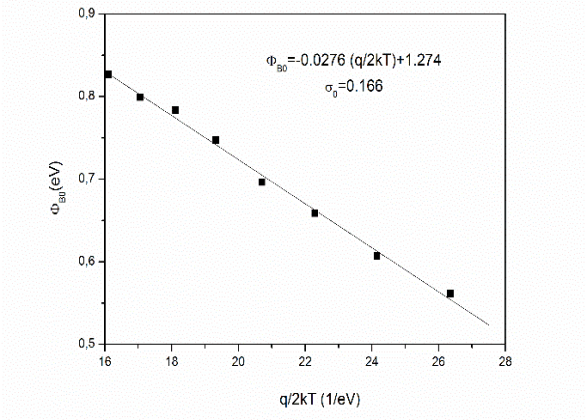

Figure 3. Plot of barrier height vs $q/2kT$ of In/SnTe/Si/Ag diode

The assumption on GD functions in barrier height expression can be related with n, and the voltage effect in n values can be formulated by the bias dependent Gaussian coefficients as,

$$\left(\frac{1}{n_{ap}} - 1\right) = -\rho_2 + \frac{q\rho_3}{2kT} \quad (7)$$

where n_{ap} is the voltage independent [13-15]. Use of $(n^{-1} - 1)$ predicts a general understanding on the dependence of n of the diode structure with inhomogeneous barrier formation in which it is expected to be inversely proportional to temperature. The barrier distribution and the identification of the voltage deformation of the this distribution can be discussed in terms of n_{ap} with the parameters, ρ_2 and ρ_3; and they also express the bias dependence of $\bar{\Phi}_{B0}$ and σ_0, respectively.

The temperature dependence of n was investigated by linear fitting of the relation observed in Fig.4. Thus, the linear relation found in $(n^{-1} - 1)$ vs $q/2kT$ plot confirms voltage deformation of the GD of the barrier height in terms of calculated n values[15]. The voltage coefficients were calculated from the slope and intercept as, $\rho_2 = 0.0346$ V and $\rho_3 = 0.0315$, respectively.

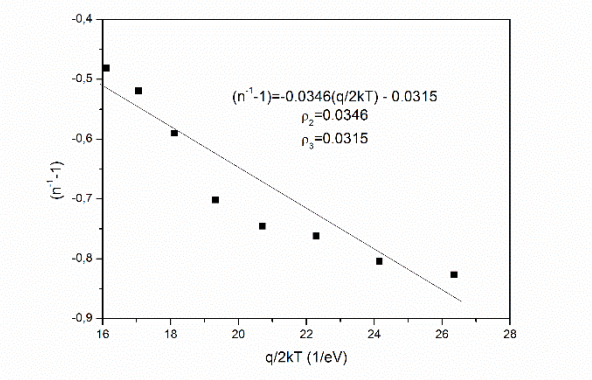

Figure 4. Plot of $(n^{-1} - 1)$ vs $q/2kT$ of In/SnTe/Si/Ag diode

The Richardson plot under the assumption of TE model deviates from linearity with the inhomogeneity of the barrier. Therefore, the value of this constant was approximated from the modified current relation given in Eq.4 as,

$$\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_s^2}{2k^2T^2}\right) = \ln(AA^*) - \frac{q\bar{\Phi}_{B0}}{kT} \quad (8)$$

According to this relation, the modified Richardson plot is presented in Fig.5. The values obtained from this analysis show a good linear relationship. The slope of the straight line directed to $\bar{\Phi}_{B0}$ and extrapolation value was used to determine A^* for a given diode area, A. The result of the fitting process in Fig.5 pointed approximately same $\bar{\Phi}_{B0}$ value as about 1.274 eV and A^* was found as 119.5 A/cm^{2}K^2 which is in close agreement with the expected value of 112 A/cm^{2}K^2 [11].

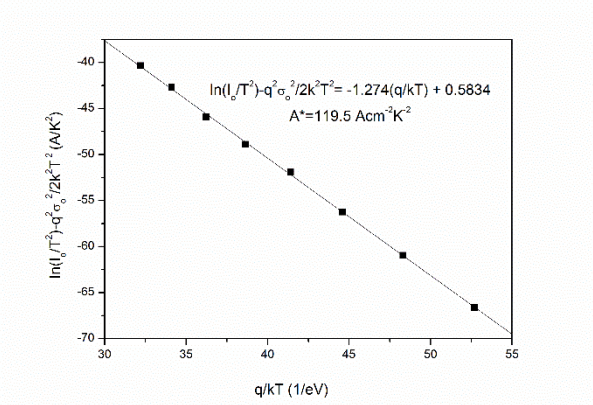

Figure 5. $\ln(I_0/T^2) - (q^2\sigma_0^2)/(2k^2T^2)$ vs q/kT of In/SnTe/Si/Ag diode

The series resistance (R_s) values that is the resistance effect in the direction of the current flow in the diode structure, were calculated with using the model proposed by Cheung and Cheung [23]. This model is used to examine the effect of R_s under the TE approximation in I-V characteristics, and this values can be expressed by Cheung's function as,

$$\frac{dV}{d(lnI)} = IR_s + n\left(\frac{kT}{q}\right) \quad (9)$$

and

$$H(I) = V - n\left(\frac{kT}{q}\right) ln\left(\frac{I}{AA^*T^2}\right) = n\Phi_{B0} + IR_s \quad (10)$$

As shown in Fig.6, both of $dV/d(lnI)$ vs I and $H(I)$ vs I plots show linear characteristics for the data of downward curvature region in the forward bias I-V. According to these two relations (Eq.9 and Eq.10), R_s values were calculated from the slope of the corresponding figures; and the temperature dependent values are listed in Table 2 and also presented in Fig.7.

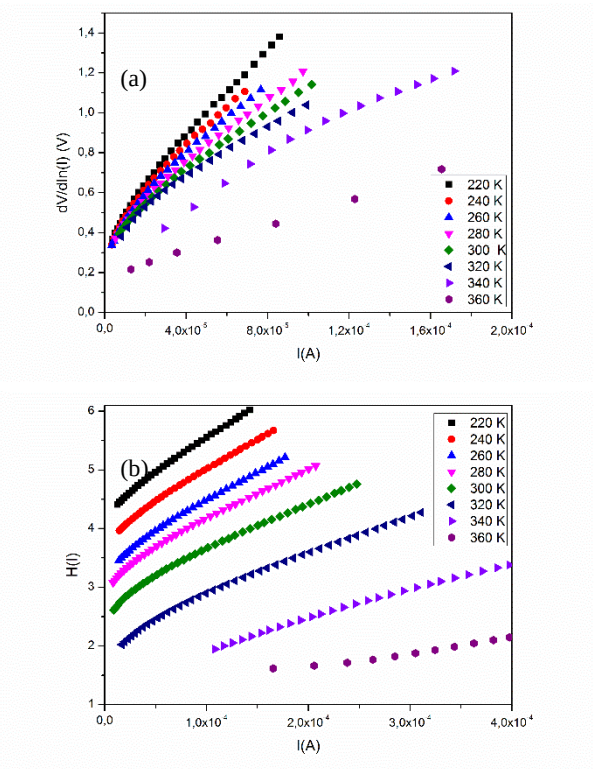

Figure 6. $dV/d(lnI)$ vs I (a) and $H(I)$ vs I (b) plots of In/SnTe/Si/Ag diode

As shown in Fig. 7, the obtained R_s are in decreasing behavior with increasing temperature. This variation in R_s values with temperature is one of the reason for increase of n and lack of free carrier concentration at low temperatures [24]. As given in this figure, the results are

Table 2. Series resistance, R_s and density of interface states, D_{it} obtained from In/SnTe/Si/Ag diode

Temperature (K)	R_s (kΩ) ($dV/dln(I)$ vs I plot)	R_s (kΩ) ($H(I)$ vs I plot)	D_{it} (eV^{-1}cm^{-2})
360	3.543	2.565	1.06x10^{13}
340	5.408	4.539	1.12x10^{12}
320	6.887	7.346	1.23x10^{13}
300	7.725	8.613	1.36x10^{12}
280	8.772	9.633	2.29x10^{13}
260	8.762	10.465	2.70x10^{13}
240	10.385	11.047	6.93x10^{12}
220	11.963	12.177	7.35x10^{13}

in a good agreement with each other and confirms the consistency of Cheung's function [23, 25].

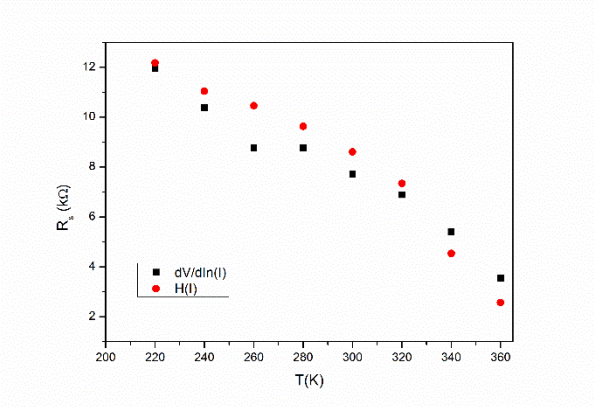

Figure 7. Plot of temperature dependent R_s values for In/SnTe/Si/Ag diode

The presence of insulator layer at the interface can be affected on the barrier height distribution in the junction [13-14] and this charge density can arise through a net charge in interface states or through mobile carriers accumulated at the junction interface [24, 25]. The interface states are determined as to exist at the Si-SiO_2 interface [26]. According to the Card and Rhoderick, the density distribution curves of the interface state D_{it} in equilibrium with the semiconductor can be determined from the forward bias I–V characteristics at each temperature [12]. Fig.8 illustrates distribution profiles of D_{it} values as a function the energy of interface states with respect to the conduction band, $E_c - E_{ss}$ for each temperature, extracted from the forward bias I–V characteristics taking into account both the bias dependence of the effective barrier height and with and without R_s obtained from the forward bias I–V characteristics of the diode. It was observed that the values of D_{it} increase with decreasing temperature [27].

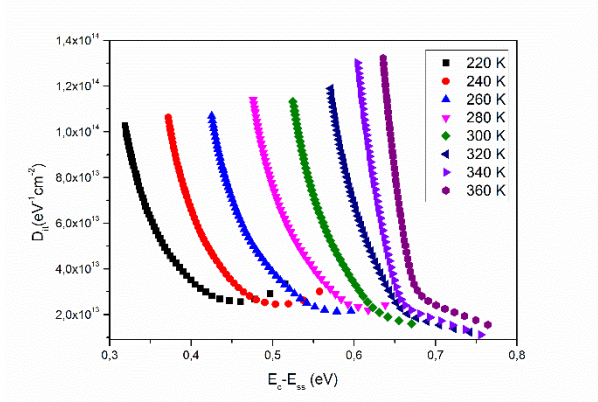

Figure 8. D_{it} as a function of $E_c - E_{ss}$ obtained from In/SnTe/Si/Ag diode

6. CONCLUSION (SONUÇ)

In this study, the temperature dependence of I-V characteristics of the In/SnTe/Si/Ag diode structure was analyzed under the assumption of GD of the barrier height to explain the temperature dependence of Φ_{B0} and n. Main diode parameters as n, Φ_{B0}, R_s and D_{it} of the fabricated diode structure were calculated from the forward bias I–V measurements. Variation in diode parameters with ambient temperature was explained by barrier inhomogeneity with low barrier patches. The distribution of the inhomogeneous barrier height was represented by the existence of Gaussian type function on barrier heights around 1.274 eV mean value. GD approach also achieved to provide a satisfactorily explanation and Richardson constant from the modified $\ln(I_0/T^2) - (q^2\sigma_0^2)/(2k^2T^2)$ vs q/kT plot, was found in a close agreement for the reported values as 119.5 A/cm^{2}K^2. R_s values were approximated by the help of Cheung's function and found in decreasing behavior with increase in temperature. In addition, taking into account of the presence of insulator layer at the junction interface, distribution profile of the density of interface states was investigated.

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